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| 09/821,442 | 03/29/2001 | Kenji Nakamura | 15162/03490 | 1740 |

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| EXAMINER | |
|---|---|
| NGUYEN, LUONG TRUNG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2612 | |

DATE MAILED: 12/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/821,442 | NAKAMURA, KENJI | |
| | Examiner | Art Unit | |
| | LUONG T. NGUYEN | 2612 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/11//05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/16/2005 has been entered.

### *Response to Arguments*

2. Applicant's arguments filed 11/16/2005 have been fully considered but they are not persuasive.

In re page 4, Applicant argues that claim 1 does in fact require a reconfigurable processing element that is not a CPU. Claim 1 recites a camera comprising

> ... an electronic circuit arrangement in which a logic circuit is obtained when a predetermined program is written, said logic circuit is configured depending on the written program, and said logic circuit executes a predetermined operation on inputted image data ...;

Thus, the camera of claim 1 requires a circuit that can be configured to form different logic circuits, wherein each logic circuit performs a predetermined operation on input image data.

In response, regarding claim 1, it is noted that the features "*a reconfigurable processing element may be used for anything other than implementing the CPU; different logic circuits, wherein each logic circuit performs a predetermined operation on input image data*" are not recited in claim 1. Instead, Applicant recited claim 1 with the limitation "an electronic circuit arrangement in which **a logic circuit** is obtained when a predetermined program is written, said logic circuit is configured depending on the written program, and said logic circuit executes a predetermined operation on inputted image data." Note that claim 1 does not require "different logic circuits," claim 1 only recites "a logic circuit." The Examiner considers that claim 1 as recited still does not distinguish from Suzuki et al. and Suzuki. Suzuki et al. discloses a CPU 34 is preferably implemented on special purpose computer, a programmed microprocessor, an ASIC or other integrated circuit elements, a hardwired electronic or logic circuit such as a discrete element circuit, a programmable logic device such as a PLD, PLA, FGPA or PAL (an electronic circuit arrangement, section [0054], page 3). In addition, it is noted that the Applicant considers the electronic circuit arrangement is a field programmable gate array as recited in claim 3.

In re page 5, Applicants argues that Suzuki '975 does not discloses a controller that copies the program from a memory to a reconfiguration circuit as required by claim 1.

In response, regarding claim 1, it is noted that the feature "a controller that copies the program from a memory to a reconfiguration circuit" is not recited in claim 1. Instead claim 1 recited the limitation "a controller for reading the first program from the memory and writing it in the electronic circuit arrangement when the first mode is selected by the mode selector and for reading the second program from the memory and writing it in the electronic circuit arrangement

when the second mode is selected by the mode selector." The Examiner considers Suzuki et al. and Suzuki ('975) do disclose this feature. Suzuki et al. discloses CPU 34 is a programmed microprocessor controls processing image data readout from CCD 20 to be recorded on memory card 24 or to be displayed on LCD 6, Page 3, Section [0054]. And Suzuki ('975) discloses a digital camera, in which an image compressing/extending means is realized by a control program stored in the CPU 113 (Column 30, Lines 21-36).

In re page 6, Applicant argues that the features of claim 8 are not disclosed, taught, or otherwise suggested by Suzuki '975 and Suzuki et al.

In response, regarding claim 8, the Applicant recited claim 8 with the limitation "an electronic circuit arrangement in which a logic circuit is obtained when a predetermined program is written, said logic circuit is configured depending on the written program, and said logic circuit executes a predetermined operation on image data input thereto; a memory for memorizing a plurality of programs corresponding to the plurality of image processing; and a controller for reading a program corresponding to the image processing selected by the image processing selector and writing it in the electronic circuit arrangement." The Examiner considers that claim 8 as recited still does not distinguish from Suzuki et al. and Suzuki. Suzuki et al. discloses a CPU 34 is preferably implemented on special purpose computer, a programmed microprocessor, an ASIC or other integrated circuit elements, a hardwired electronic or logic circuit such as a discrete element circuit, a programmable logic device such as a PLD, PLA, FGPA or PAL (an electronic circuit arrangement, section [0054], page 3). And Suzuki ('975) discloses a digital camera, in which an image compressing/extending means is realized by a

control program stored in the CPU 113 (Column 30, Lines 21-36). In addition, it is noted that the Applicant considers the electronic circuit arrangement is a field programmable gate array as recited in claim 11.

In re pages 7-8, Applicant argues that Tomaszewski merely teaches a camera that determines if it is connected to a computer, but does not detect how it is connected, e.g., by USB and RS-232).

In response, regarding claim 4, the Applicant recited in claim 4 the limitation "a detector for judging a kind of data communication standard of an equipment connected to the connection portion." The Examiner considers that Tomaszewski does disclose this feature. Tomaszewski discloses the USB connectivity is detected by the presence of the VBUS signal 210, which is detected by VBUS signal checker 500 (Figures 4-5, Page 2, Section [0029] through Section [0034]); the USB is a kind of data communication standard of an equipment.

In re pages 7-8, Applicant argues that Tomaszewski does not even mention a second communication standard, it is nonsensical to hold that it teaches to distinguish between two different communication standards. It is respectfully submitted that all of the other references, i.e., Clemens, Suzuki et al, and Anderson, also fail to teach this feature of claim 4.

In response, regarding claim 4, Applicant recited the limitation "a connection portion to which a first equipment and a second equipment can alternatively be connected, the first equipment being communicative with the camera by a first data communication standard, and the second equipment being communicative with the camera by a second data communication

standard." The Examiner considers that claim 4 as recited still does not distinguish from Tomaszewski in view of Clemens (WO 99/40723) and Suzuki et al. further in view of Anderson et al. Tomaszewski does not disclose the second equipment, which can alternatively be connected to the connection portion. However, Tomaszewski discloses USB serial port 107, Figure 3A, Page 2, Section [0024] as corresponds to "a connection portion." And Clemens discloses an apparatus in which the digital camera 10 is tethered to the computer 12 by a Universal Serial Bus USB or RS-232 serial interface (Figure 1, Page 8). This indicates that there are "a first equipment" and "a second equipment," which can be alternatively connected to digital camera 10, one by Universal Serial Bus USB, the other by RS-232.

In re page 8, Applicant argues that claim 4 also requires "...an electronic circuit arrangement in which a logic circuit is obtained when a predetermined program is written, said logic circuit is configured depending on the written program, and said logic circuit executes a predetermined operation on inputted image data...." This feature of claim 4 is not taught or suggested by Suzuki et al.

In response, the examiner considers that Suzuki et al. does disclose this feature as discussed above regarding claim 1.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 8, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U. S. 2002/0057351) in view of Suzuki (U. S. Patent No. 6,380,975).

Regarding claim 1, Suzuki et al. discloses a camera comprising a mode selector (Figure 12 shows that the user can select mode, such as recording mode, playback mode) for selecting one of a first mode (recording mode, Figure 12, Page 7, Section [0112]) for executing first image data processing (processing image data by DSP 33, compression/expansion circuit 38, buffer memory 37, memory card 24, Figure 4, Page 7, Section [0112]) to an image data taken by an image pickup device (CCD 20, Figure 4) and a second mode (playback mode, Figure 12, Page 7, Section [0112]) for executing second image data processing contents of which are different from that of the first image data processing (image data recorded in memory card is read out through buffer memory, compression/expansion circuit 38, LCD 6, Figure 4, Page 7, Sections [0056], [0112]); an electronic circuit arrangement in which a logic circuit is obtained when a predetermined program is written, said logic circuit is configured depending on the written program, and said logic circuit executes a predetermined operation on inputted image data (programmable logic device such as PLD, PLA, FGPA, PAL, Page 3, Section [0054]).

Suzuki et al. fails to specifically discloses a memory for memorizing a first program corresponding to the first image data processing and a second program corresponding to the second image data processing; and a controller for reading the first program from the memory and writing it in the electronic circuit arrangement when the first mode is selected by the mode selector and for reading the second program from the memory and writing it in the calculator when the second mode is selected by the mode selector. However, Suzuki et al. discloses CPU

34 is a programmed microprocessor controls processing image data readout from CCD 20 to be recorded on memory card 24 or to be displayed on LCD 6, Page 3, Section [0054]. And Suzuki ('975) discloses a digital camera, in which an image compressing/extending means is realized by a control program stored in the CPU 113 (Column 30, Lines 21-36). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Suzuki et al. by the teaching of Suzuki ('975) in order to execute compression or expansion by program. This improves operability and convenience in data transfer from a digital camera to an external device (Column 30, Lines 12-14).

Regarding claim 2, Suzuki et al. discloses the first mode is an image pickup mode for taking an image data by photoelectric transferring an optical image of an object (recording mode, CCD 20 electrically converts the light image into image signals; the image signals are recorded on memory card 24 via compression circuit 38, Figures 4, 12, Page 7, Section [0112]); the second mode is a reproducing mode (playback mode, Figures 4, 12, Page 7, Section [0112]) for reproducing an image on a display (LCD 6, Figure 4, Page 3, Section [0056]) by using an image data taken by the image pickup mode; the first image data processing is a data compression processing of the image data taken by the image pickup mode (compression in compression/expansion circuit 38, Figure 4, Page 3, Section [0051]); and the second image data processing is a data extension processing of a compressed image data (expansion in compression/expansion circuit 38, Figure 4, Page 3, Section [0056]).

Regarding claim 3, Suzuki et al. discloses the electronic circuit arrangement is a field programmable gate array FGPA, Page 3, Section [0054]).

Regarding claim 8, Suzuki et al. discloses a camera comprising an image processing selector for selecting an image processing among a plurality of image processing corresponding to different characteristics with respect to quality of an image (Figure 12 shows that the user can select mode, such as image processing for recording mode or playback mode); an electronic circuit arrangement in which a logic circuit is obtained when a predetermined program is written, said logic circuit is configured depending on the written program, and said logic circuit executes a predetermined operation on inputted image data (programmable logic device such as PLD, PLA, FGPA, PAL, Page 3, Section [0054]).

Suzuki et al. fails to specifically disclose a memory for memorizing a plurality of programs corresponding to the plurality of image processing; and a controller for reading, a program corresponding to the image processing selected by the image processing selector and writing it in the electronic circuit arrangement. However, Suzuki et al. discloses CPU 34 is a programmed microprocessor controls processing image data readout from CCD 20 to be recorded on memory card 24 or to be displayed on LCD 6, Page 3, Section [0054]. And Suzuki ('975) discloses a digital camera, in which an image compressing/extending means is realized by a control program stored in the CPU 113 (Column 30, Lines 21-36). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Suzuki et al. by the teaching of Suzuki ('975) in order to execute compression or

expansion by program. This improves operability and convenience in data transfer from a digital camera to an external device (Column 30, Lines 12-14).

Regarding claim 11, Suzuki et al. discloses the electronic circuit arrangement is a field programmable gate array FGPA, Page 3, Section [0054]).

5. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomaszewski (US 2001/0001563) in view of Clemens (WO 99/40723) in view of Suzuki et al. (U. S. 2002/0057351) further in view of Anderson et al. (U. S. Patent No. 6,567,122).

Regarding claim 4, Tomaszewski discloses a camera comprising a connection portion (USB serial port 107, Figure 3A, Page 2, Section [0024]) to which a first equipment (USB cable 106, Figure 3A, Page 2, Section [0024]), the first equipment being communicative with the camera by a first data communication standard; a detector for judging a kind of data communication standard of an equipment connected to the connection portion (the USB connectivity is detected by the presence of the VBUS signal 210, which is detected by VBUS signal checker 500, Figures 4-5, Page 2, Section [0029] through Section [0034]); a controller (camera manager 501, Figure 5, Section [0029] through Section [0034]) for reading the first program from the memory and writing it in the electronic circuit arrangement when the kind of the data communication standard of the equipment connected to the communication portion is judged as the first data communication standard by the detector.

Tomaszewski fails to disclose a second equipment and the second equipment being communicative with the camera by a second data communication standard; reading a second

program from the memory and writing it in the electronic circuit arrangement when the kind of the data communication standard of the equipment is judged as the second data communication standard. However, Clemens discloses an apparatus in which the digital camera 10 is tethered to the computer 12 by a Universal Serial Bus USB or RS-232 serial interface (Figure 1, Page 8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Tomaszewski by the teaching of Clemens in order to connect a digital camera to a computer by using different type of bus.

Tomaszewski and Clemens fail to disclose an electronic circuit arrangement in which a logic circuit is obtained when a predetermined program is written, said logic circuit is configured depending on the written program, and said logic circuit executes a predetermined operation on inputted image data. However, Suzuki et al. discloses an electronic camera, which comprises a CPU 34 which is preferably implemented a programmed logic device, such as PLD, PLA, FGPA, PAL, section [0054], page 3. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Tomaszewski and Clemens by the teaching of Suzuki et al. in order to control the operation of the camera.

Tomaszewski, Clemens and Suzuki et al. do not disclose a memory for memorizing a first program corresponding to a first image data communication processing fitting for the first data communication standard and a second program corresponding to a second image data communication processing fitting for the second data communication standard. However, Anderson et al. discloses a digital camera, in which an application software for operating USB connection is stored in DRAM 346, Figures 3, 9, Column 12, Lines 23-40). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

modify the device in Tomaszewski, Clemens and Suzuki et al. by the teaching of Anderson et al. in order to store program for controlling connection between a digital camera and a computer.

Regarding claim 5, Clemens discloses the first data communication standard and the second data communication standard are respectively a USB standard and an RS-232C standard (Page 8).

Regarding claim 6, Tomaszewski discloses wherein the equipment to be connected to the connection portion is an equipment which can execute an image data processing (Page 1, Section [0021].

Regarding claim 7, Suzuki et al. discloses the electronic circuit arrangement is a field programmable gate array (PGPA, Page 3, Section [0054].

6. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U. S. 2002/0057351) in view of Suzuki (U. S. Patent No. 6,380,975) further in view of Nakamura (U. S. Patent No. 6,278,492).

Regarding claim 9, Suzuki et al. and Suzuki ('975) fail to specifically disclose the image processing with respect to the quality of the image is a gamma compensation. However, Suzuki et al. discloses the digital signal processor DSP 33 processes image data and supplies image data to memory card 24 via buffer memory 37, Figure 4, Page 3, Section [0051]. And Nakamura discloses a camera, in which image signal output from A/D conversion circuits 15R, 15G and

15B are sent to digital processing circuit 16, which processes the image signals with digital signal processing such as gamma processing (Column 4, Line 65 – Column 5, Line 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Suzuki et al. and Suzuki ('975) by the teaching of Nakamura in order to improve the quality of the image data.

Regarding claim 10, Suzuki et al. and Suzuki ('975) fail to specifically disclose the image processing with respect to the quality of the image is a contour emphasizing or unemphasizing compensation of the image. However, Suzuki et al. discloses the digital signal processor DSP 33 processes image data and supplies image data to memory card 24 via buffer memory 37, Figure 4, Page 3, Section [0051]. And Nakamura discloses a camera, in which image signal output from A/D conversion circuits 15R, 15G and 15B are sent to digital processing circuit 16, which processes the image signals with digital signal processing such as contour enhancement (Column 4, Line 65 – Column 5, Line 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Suzuki et al. and Suzuki ('975) by the teaching of Nakamura in order to improve the sharpness of the image data.

***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NGOCYEN VU can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LN
11/30/05

Luong Nguyen

LUONG T. NGUYEN
PATENT EXAMINER